

MULTI-DRIVE BANDWIDTH EXTENDED STACKED AMPLIFIER IN SIGE:C130 NM BICMOS TECHNOLOGY

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Abstract

A multi-drive broadband stacked distributed amplifier along with simulations and design in SiGe:C BiCMOS 130nm technology, has been presented in this work. The proposed multi-drive stacked distributed amplifier (MD-SDDA) consists of four devices implemented in a unit-stack topology. The unit-stack utilizes multi-drive technique by coupling the signal from previous unit-stack to the base of common-base device of the next unit-stack. Additionally, the top most device in the unit-stack is deployed as cascode to mitigate the stability issue arising from the forward coupling between inter-stacks. There are three unit-stacks implemented in a uniform distributed topology out of which two unit-stacks employ multi-drive technique. The device sizes are kept same to increase the impedance moving up in the stack and to ease the device biasing. Small-signal simulations of the proposed MD-SDDA design demonstrate 135THz of Gain-bandwidth product (GBW) with 20 dB gain. The average group delay is ± 10 psec with a variation of ± 3.5 psec throughout the entire operating band stating the effectiveness of proposed design for a broadband signal. Total harmonic distortion (THD) of 5% at output power of 16 dBm identifies the suitability of the approach for higher modulation formats towards realizing data rates as high as 800 Gbps. Lastly, the proposed MD-SDDA is compared with a conventional stacked distributed amplifier (SDDA) under the same number of unit-stacks, devices in the unit-stacks, and DC bias conditions. The proposed MD-SDDA yields superior gain-bandwidth product of 135 THz as compared to 109 THz for a conventional SDDA.

1. INTRODUCTION

Broadband amplification is the most important and fundamental requirement of any data-demanding wireless/wired communication system. The applications such as high-definition video, cloud computing, data centers where data traffic is not

only in large volumes but also increasing further to accommodate the modern applications [1][2]. For such applications, broadband amplification is required to compensate for the signal attenuation by providing reasonable gain over the operating bandwidth.

Distributed amplifiers (DA) topology present a viable solution for broadband amplification. In distributed amplifiers topology, the devices are placed in a distributed fashion. The input capacitance along with series inductors form the artificial transmission lines that are utilised to feed the input signal. Resultingly, the generated output current from the devices is delivered additively to the output artificial transmission lines formed between the series inductors and output capacitance. The output current collected from the devices is accumulated into the load to form the output power. Ideally, infinite number of devices can be distributed on these artificial transmission lines enabling the distributed amplifier to have infinite gain bandwidth product [3].

Despite the above advantages, conventional DAs topology struggle to generate enough gain firstly, because of the additive gain mechanism and secondly, half of the generated currents are terminated in the idle terminations. Cascading DAs [4]–[10] increases the gain however, the achievable bandwidth is somewhat compromised because of the additional bandwidth limiting poles introduced. Similarly, the non-uniform topology ensures that the output currents from the devices travel only towards the load rather than the half of that current wasted in idle-termination, thus, raising the output power delivered to the load [11]–[13]. Since, the idle-termination is removed, this approach also results in lower operating bandwidths.

One possible solution is to enhance the current contribution of each device by increasing the device sizes, however, resulting increase in parasitic capacitances lowers the cut-off frequency of the transmission lines. Stacked topology offers an effective approach for obtaining high output voltage swings and hence output power over narrowband operation [14]–[21]. This approach was extended to wideband distributed implementations in [22]–[23]. Stacking devices deployed in distributed architecture enables high output power over wideband. The stacked active devices shares a portion of the total voltage swing

generated at the top of the stack while the total swing is referred from the top of the stack to the ground.

Multi-drive stacked DAs have provided 100 mW output power over 100 GHz bandwidth on a Silicon-On-Insulator (SOI) platforms [25]–[27]. In multi-drive stacking, all devices in the stack contribute to output voltage swing, thus offering larger gain and higher output voltage swings as compared to the conventional stacked distributed amplifiers.

This work presents a bandwidth extended multi-drive stacked distributed amplifier. The proposed topology employs multi-drive technique in two of the three unit-stacks. Meanwhile, each unit-stack is modified to increase the output impedance and input-output isolation. The proposed amplifier is implemented in an IHP SG13G2 technology with f_t/f_{max} of 350/450 GHz. Further, there is also possibility of integration of CMOS and HBTs on the same platform in this technology that leads to cost effective and compact solution for very high data rate applications.

2. BANDWIDTH EXTENSION TECHNIQUES

The bandwidth limitation arises from parasitic capacitances kicking in at the intermediate to high frequencies. There are various bandwidth extension techniques found in the literature such as series inductive peaking, shunt inductive peaking, double series shunt inductive peaking etc to tune out the effect these parasitics and enabling the design to operate at higher frequencies [28]. In conventional SDDAs, the artificial transmission lines formed between series inductors and input/output parasitic capacitances offer higher cut-off frequencies and do not limit the operating bandwidth. Inter-stage parasitic capacitances in the unit-stack and loss on the input-output artificial lines are the two critical components that define the operating bandwidth of the SDDA designs. Therefore, the bandwidth extension techniques utilized should cater for both the aforementioned limitations.

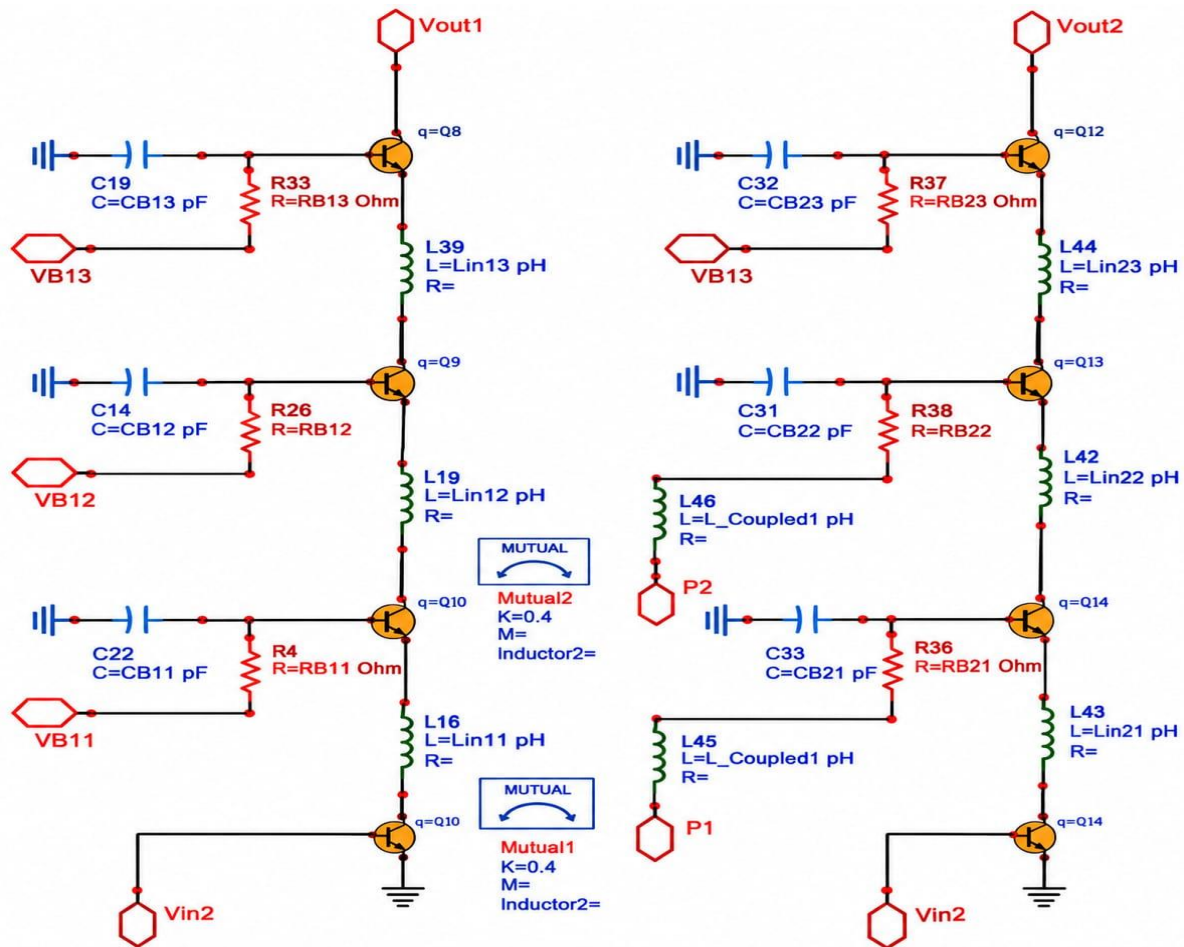


Figure 1: Multi-drive broadband Unit-Stack Cell

3. MULTI-DRIVE UNIT-STACK

Multi-drive unit-stack offers distinct advantages over a conventional unit-stack in number of ways. In conventional stacking, devices are stacked on top to generate higher output voltage swings at the top, resulting in high output power. There are two components of AC current swing " i_c " generated at the collector of the common-emitter device, one component flows towards the emitter of the common-base device in the stack while the other component is coupled to the base of the same device and is eventually dissipated in the base resistance [25]–[27]. This lost current component can be compensated by injecting additional current into the base of the common-base device. The additional current can be coupled from the

collector current flowing in the previous adjacent unit-stack cell. Furthermore, the coupling can be adjusted in the design to compensate the losses occurring at higher frequencies. Although, this technique is very effective yet it has some drawbacks. The coupling occurs at the base of common-base device through a series inductance deployed at the base. This introduces a negative resistance seen from the collector/output node that helps in reducing the high frequency losses. However, the input-output isolation suffers and the amplifier becomes unstable. Therefore, this technique is modified by introducing a cascode at the top of stack to increase the input-output isolation. Additionally, this also enhances the output impedance, thus increasing the overall gain

as well. Thus, the proposed multi-drive broadband unit-stack not only compensates the loss at higher frequencies but also resolves the stability issue. $Q_{1,2}$ are the common emitter devices while $Q_{3,4}$ and $Q_{5,6}$ are the common base devices. $Q_{7,8}$ are placed as cascode on top of the proposed stack. Inter-stack coupling occurs between inductors L_{16} and L_{45} with

coupling coefficient of “K”. Similarly, the second inter-stack coupling is performed through L_{19} and L_{46} inductors whereas peaking within stack is performed through series inductors L_{int11} , L_{int12} , L_{int13} , L_{int21} , L_{int22} and L_{int33} . The complete proposed multi-drive unit-stack is depicted in Figure [1].

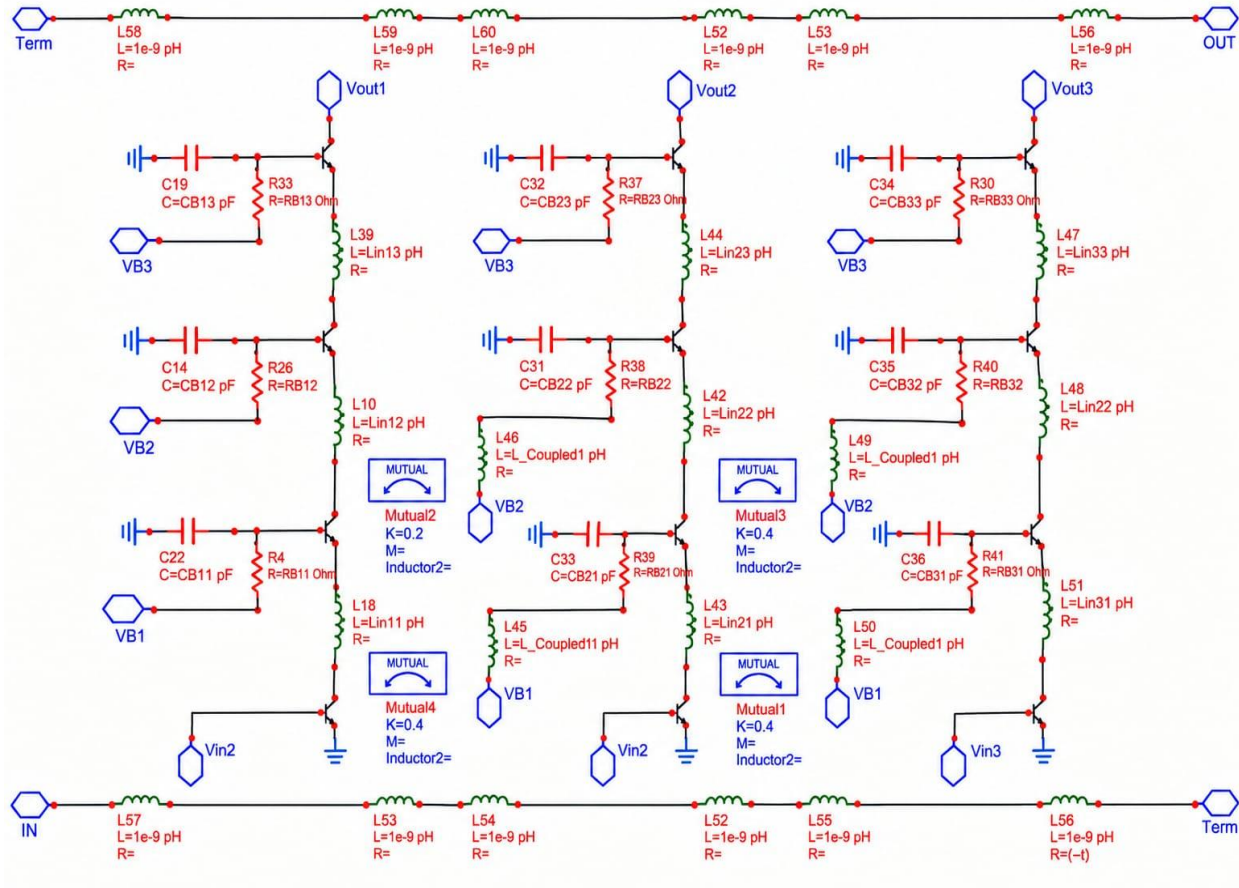


Figure 2: Complete design of the proposed multi-drive bandwidth extended stacked distributed amplifier

Table I. Device Sizes in the Multi-Drive Unit-Stack

Device	Sizes
Q_1	4 X 70 X 900 nm
Q_2	4 X 70 X 900 nm
Q_3	4 X 70 X 900 nm
Q_4	4 X 70 X 900 nm

4. PROPOSED SDDA COMPLETE DESIGN WITH MULTI-DRIVE BROADBAND UNIT-STACK

The broadband multi-drive unit-stack is deployed in a uniform distributed topology. The artificial transmission lines are modelled as series inductor and the shunt capacitance from the devices. Series inductor L_B and shunt parasitic capacitance C_{in} form the artificial base transmission line whereas series inductor L_C and shunt parasitic capacitance C_{out} form the artificial collector transmission line. These artificial transmission lines cut-off frequencies ($f_{CB} = 1/2\pi\sqrt{L_B C_{in}}$), ($f_{CC} = 1/2\pi\sqrt{L_C C_{out}}$) are relatively high and do not limit the obtainable bandwidth of the design. Meanwhile, four devices are deployed in the unit-stack while the voltage drop across each of the device along with the drop across the resistor establishes the maximum DC supply voltage. Assuming R_{opt} seen at the collector of common-base device, placing four devices in the stack would yield $4 \cdot R_{opt}$ at the top of stack. Such high impedance not only enhances the output voltage swing but also helps in matching the output impedance to the load, thus by reducing the mismatch losses at the artificial collector transmission line. Furthermore, the input-output capacitances of the unit-stack cell are extracted throughout the entire operating frequency. These extracted capacitances placed along with the series inductances are modelled as 50Ω that is matched to the load impedance. Additionally, the delay on the base and collector artificial lines is matched by equating the phase velocities to entertain the in-phase addition of currents between the collector nodes and collector line.

There are three unit-stacks deployed in the distributed topology out of which two unit-stacks are multi-drive stacks. The first inter-stack coupling is performed between the inductors L_{11} , L_{45} and L_{10} , L_{46} with a coupling coefficient $K = 0.2$. The second inter-stack coupling happens between the inductors L_{43} , L_{50} and L_{42} , L_{49} , respectively with coupling coefficient $K = 0.4$. Another distinct advantage of inter-stack coupling through this approach is that it becomes more effective at high frequency where additional drive signal is actually required to compensate for high

frequency losses. The drive signals are further established between the capacitance C_B and parasitic capacitance C_{BE} forming a voltage divider at the base of each device. Same scenario occurs at the base of all common-base devices contributing to the output voltage swings at the collector nodes of each respective devices. The complete schematic of the proposed multi-drive stacked distributed amplifier is depicted in Figure [2] whereas the device sizes, inductors and capacitances values are tabulated in Table II.

5. SIMULATION RESULTS AND DISCUSSIONS

The proposed design is implemented in IHP SG13G2 technology with f_t/f_{max} of 350GHz/500GHz respectively. The design is characterised through small-signal simulations to extract the small-signal gain and 3dB bandwidth. The design delivers simulated gain of >20 dB over a bandwidth of 135.4 GHz yielding to a simulated Gain-Bandwidth (GBW) of 1.35THz. The input-output Return Losses (RL) are better than 4dB throughout the entire bandwidth whereas the input-output isolation is better than 40dB. Such high isolation illustrates the effectiveness of the proposed approach. The complete small-signal performance is shown in Figure [3]. Moreover, stability simulation is performed with the Rollet-stability factor (K) is plotted and shown in Figure [4]. As can be seen, the K factor is greater than 1 over the entire range which renders further the suitability of the proposed approach. The average group delay is around 10 psec with a variation of ± 3.5 psec in the entire operating frequency band. The large-signal performance is analysed with Harmonic Balance simulations. Maximum output power versus the input power, is simulated at 1 GHz to capture the non-linearities occurring due to the harmonics spanning over the operational bandwidth. The proposed design delivers saturated output power of 16–17 dBm. Further, the output power can be increased by increasing the DC supply voltage. The linearity performance of the proposed design is also characterized through Harmonic Balance simulation by calculating the total harmonic distortion (THD) at 1 GHz.

Table II. Parameters and device sizes of the proposed SDDA bandwidth extended design

Device	Sizes
Q_1	3 X 70 X 900 nm
Q_2	4 X 70 X 900 nm
Q_3	2 X 70 X 900 nm
Q_4	2 X 70 X 900 nm
L_B	30 pH
L_C	100 pH
L_{RFC}	10 nH
R_C (Collector Term)	80 Ω
R_b (Base Term)	50 Ω
R_L	50 Ω
V_{b0}	0.9 V
V_{b1}	2 V
V_{b2}	3.3 V
V_{b3}	4.2 V
V_{CC}	4.8 V
C_{B11}	0.25 pF
C_{B12}	0.25 pF
C_{B13}	0.2 pF
R_{B11}	500 Ω
R_{B12}	500 Ω
R_{B13}	100 Ω
C_{B21}	0.25 pF
C_{B22}	0.25 pF
C_{B23}	0.2 pF
R_{B21}	10 Ω
R_{B22}	10 Ω
R_{B23}	100 Ω
C_{B31}	0.25 pF
C_{B32}	0.25 pF
C_{B33}	0.2 pF
R_{B31}	10 Ω
R_{B32}	10 Ω
R_{B33}	100 Ω
Coupling coefficient K1	0.2
Coupling coefficient K2	0.4

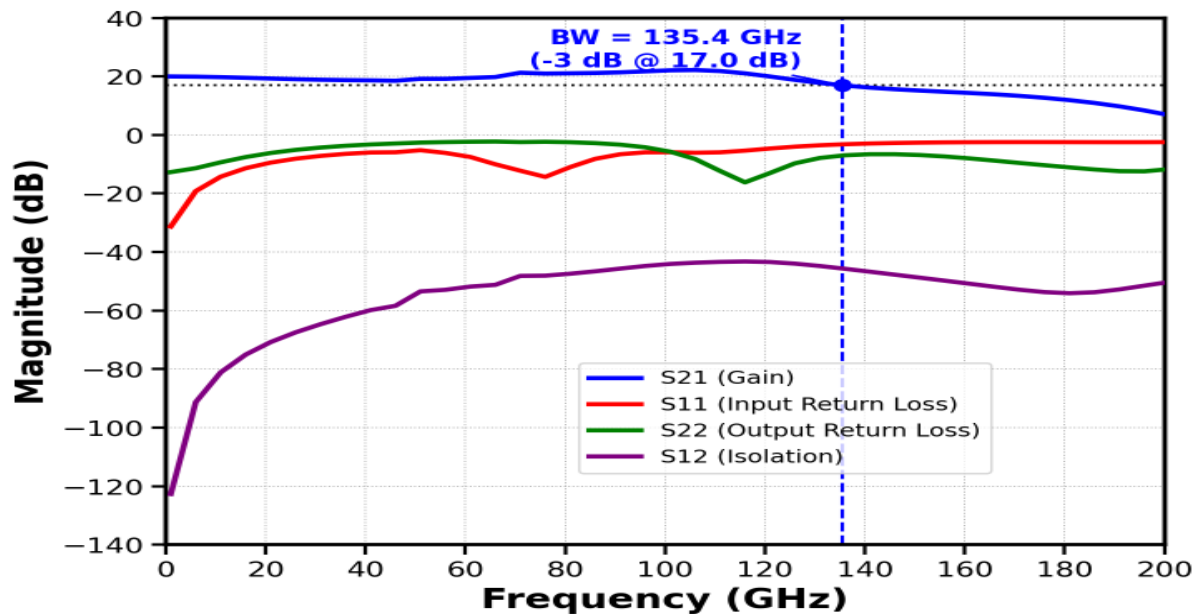


Figure 3: Simulated S-parameters of the proposed bandwidth extended multi-drive distributed power amplifier

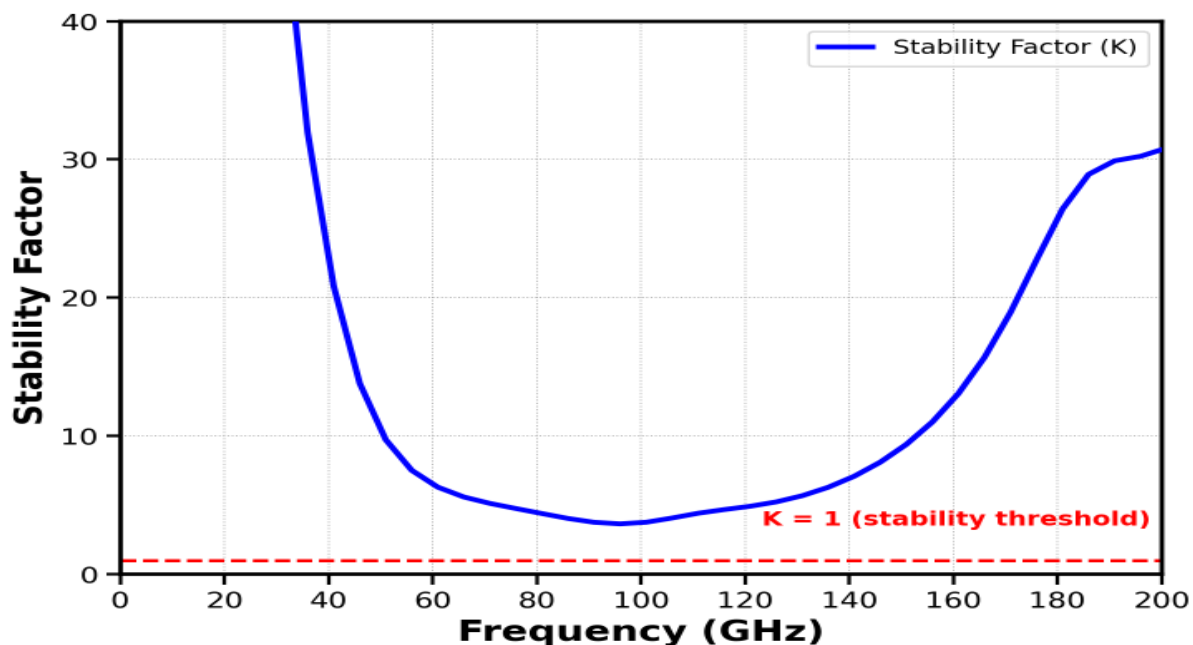


Figure 4: Simulated stability factor of the bandwidth extended multi-drive distributed power amplifier

The total harmonic distortions can be defined as

$$THD = \frac{\text{Power in Harmonics Frequencies}}{\text{Power in the Fundamental Frequency}}$$

The large-signal simulated performance of the bandwidth extended multi-drive distributed power amplifier is depicted in Figure [6].

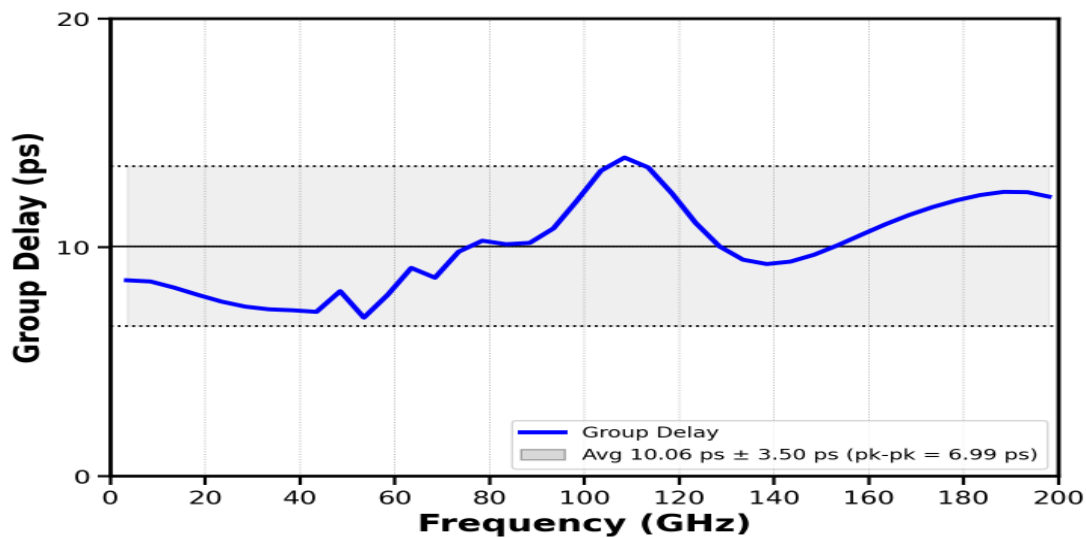


Figure 5: Simulated group delay of the proposed bandwidth extended multi-drive distributed power amplifier

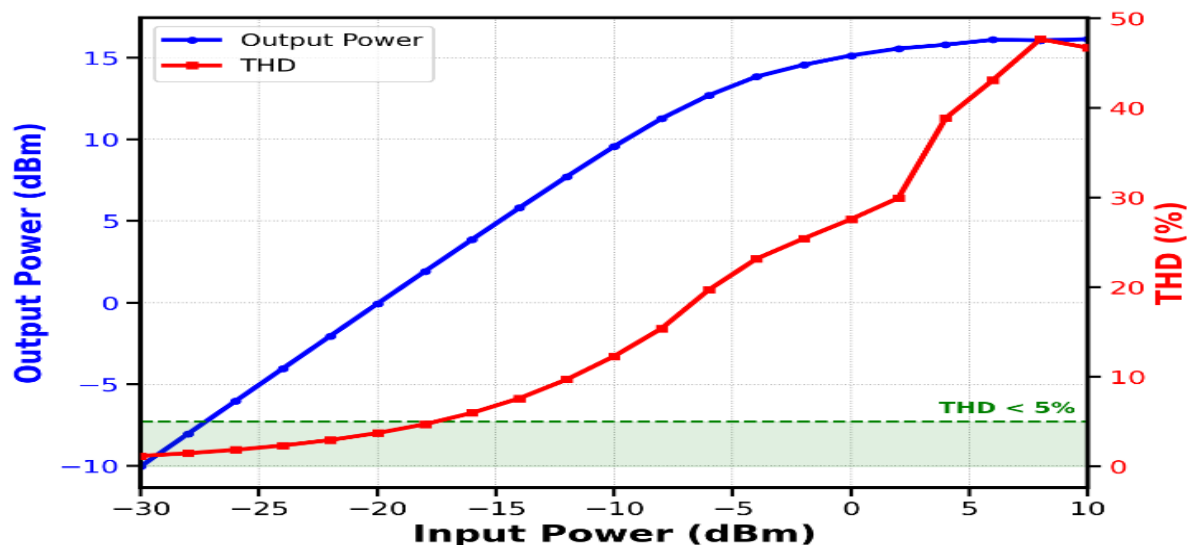


Figure 6: Simulated output power and THD of the proposed bandwidth extended multi-drive distributed power amplifier

6. COMPARISON OF THE PROPOSED DESIGN WITH A CONVENTIONAL STACKED DISTRIBUTED AMPLIFIER

The proposed bandwidth extended multi-drive design has been compared with a conventional stacked distributed power amplifier under the same scenario. The conventional stacked distributed amplifier consists of three devices in the unit-stack

with three number of unit-stacks in the design. Further, the device sizes along with the DC operating points are kept the same for both designs. The DC current flowing from the supply is similar to the one in proposed bandwidth extended design. Figure [7] demonstrates the comparison of the small-signal performance of the two designs. The simulated 3dB bandwidth for the proposed design

is 135THz while for the conventional design is 109 THz, demonstrating the effectiveness of the proposed approach. Additionally, current waveforms at the base of common–base device in the last unit–stack have been simulated and shown in Figure [8]. The current waveform for the case of proposed multi–drive stacked amplifier is almost twice as compared to the one for conventional stacked power amplifier design, courtesy to multi–

drive technique. Meanwhile, it should also be noted that the current waveforms are simulated at 120 GHz where a dip in the gain can be seen in simulated small–signal performance. That stems from the fact that at high frequency conventional stacked distributed amplifier suffers from losses which are compensated by the proposed approach and hence the operational bandwidth is enhanced.

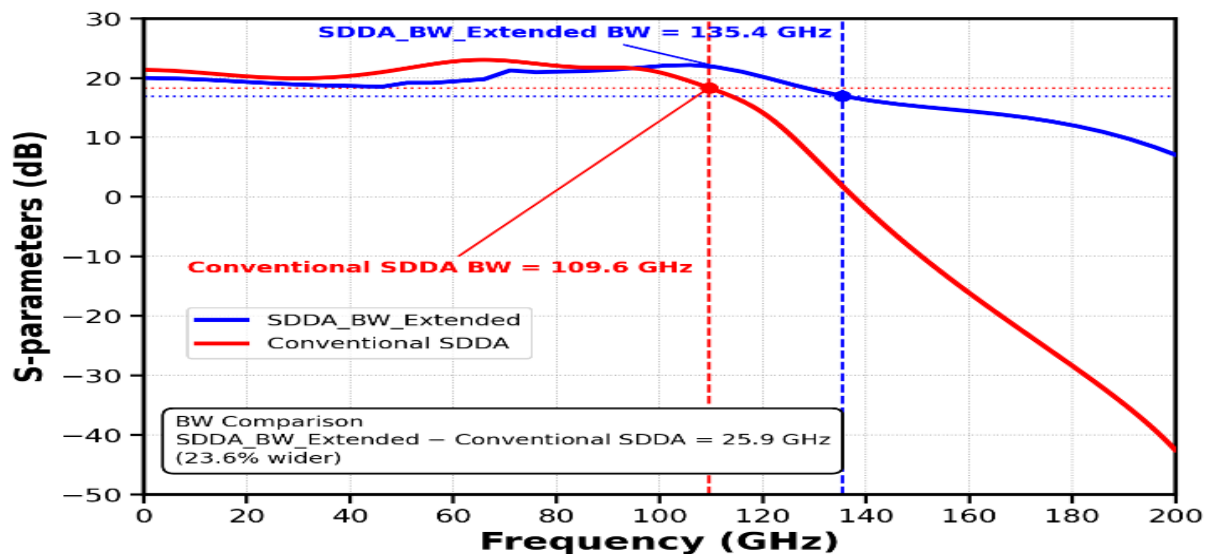


Figure 7: Comparison of the small–signal performance of the proposed multi–drive stacked DA with conventional stacked DA with same number of unit–stacks and DC biasing

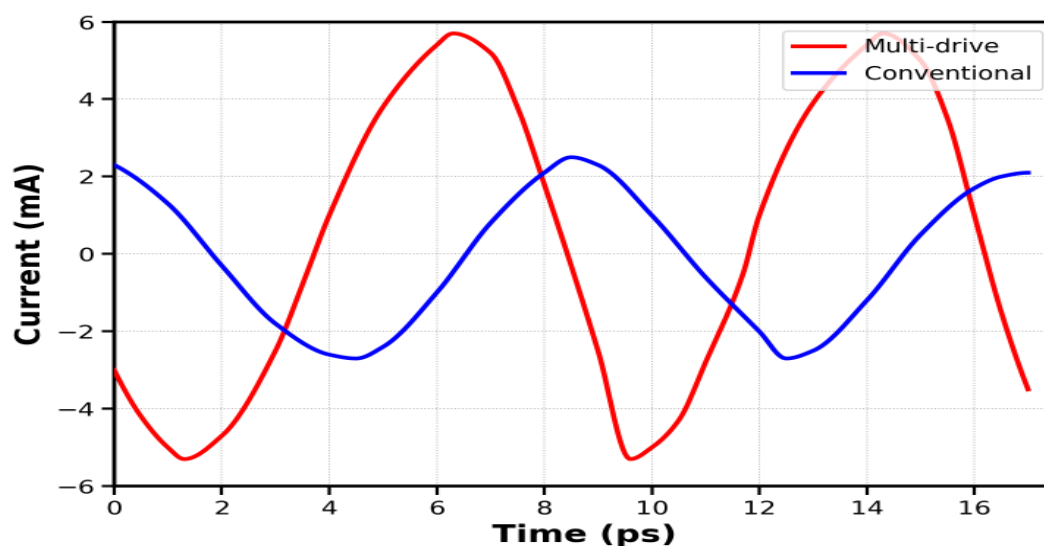


Figure 8: Comparison of the AC base current at common–base in the unit–stack of the multi–drive stacked DA and the conventional DA

7. CONCLUSION

This work describes a broadband multi-drive stacked distributed amplifier delivering 20 dB gain over 135 GHz of bandwidth, resulting into 1.35 THz of Gain-Bandwidth Product. The proposed design employs multi-drive stacking approach to compensate for the losses occurring at high frequency through inter-stack coupling. Further, the multi-drive unit-stack is modified by introducing a cascode at the top to ensure the input-output isolation. The input-output reverse

isolation (S_{12}) lower than 40dB is achieved in the small-signal simulation. Such high GBW enables the design to achieve data rates as high as 190 to 200 Gbps with the simplest of modulation, for instance, ON-OFF-KEYING (OOK) [29]. The linearity performance, THD = 5% at output power of 5 dBm, suggests that the design has the capability to support 400 Gbps, 800 Gbps of data rate if higher modulation formats are utilized.

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